Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **INPUT B3**
2. **INPUT A<B**
3. **INPUT A=B**
4. **INPUT A>B**
5. **OUTPUT A>B**
6. **OUTPUT A=B**
7. **OUTPUT A<B**
8. **GND**
9. **INPUT B0**
10. **INPUT A0**
11. **INPUT B1**
12. **INPUT A1**
13. **INPUT A2**
14. **INPUT B2**
15. **INPUT A3**
16. **VCC**

**.048”**

**.050”**

**1 16**

**2**

**3**

**4**

**5**

**6**

**7**

**15**

**14**

**13**

**12**

**11**

**8 9 10**

**LS85**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: LS85**

**APPROVED BY: DK DIE SIZE .048” X .050” DATE: 11/1/17**

**MFG: MOTOROLA THICKNESS .012” P/N: 54LS85**

**DG 10.1.2**

#### Rev B, 7/1